DETAILED ACTION

Specification

1. The Examiner acknowledges the amendment(s) to the abstract filed on June 17, 2009. The objection(s) to the abstract cited in the previous office action filed on March 17, 2009 is (are) hereby withdrawn.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Layered Semiconductor Device with Metallic Electrodes.

Claim Rejections - 35 USC § 112

3. The Examiner acknowledges the amendment(s) to claim 14 filed on June 17, 2009. The rejection of claim(s) 14 under USC 112, second paragraph, cited in the previous office action filed on March 17, 2009 is (are) hereby withdrawn.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 7, 14, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki et al. (US 6,013,930, prior art of record).

a. Regarding claim 1, **Yamazaki discloses a semiconductor device** (e.g. figures 1A – 2B and 5A – 5C) **comprising:**

a first electrode component (source electrode 501);

a second electrode component (drain electrode 502);

a first layer comprising at least a portion of the first electrode component and at least a portion of the second electrode component (e.g. top layer comprising first and second electrode components 501 and 502);

a second layer having a portion comprising deposited semiconductor material contacting the first and second electrode components (second layer comprising semiconductor material 503 and the remaining semiconductor layer 111, disclosed in col. 14, lines 30 – 33 and col. 12, lines 25 – 27); **and**

a third layer comprising a substrate (substrate 101),

wherein the first, second and third layers are arranged in order such that the second layer is positioned between the first layer and the third layer (e.g. as seen in figure 1, second layer comprising layers 111 and 503 is between first layer comprising components 501 and 503, and third layer 101) **and**

wherein the first and second electrode components comprise electro-deposited metal (e.g. col. 11, lines 58 - 62 disclose the first and second

electrode components (source and drain electrodes) are made of titanium and aluminum. Regarding the limitation "*electro-deposited*", the patentability of a product does not depend on the method of production. See MPEP 2113. The electrode components are metal (titanium and aluminum) and therefore anticipate the structural limitation, regardless of how that structure is formed),

wherein the device is a thin film transistor (e.g. as disclosed in col. 14, line 18) **having a channel in the semiconductor material** (e.g. channel region 503, disclosed in col. 14, line 33), **a source electrode as the first electrode** (source electrode 501, disclosed in col. 14, lines 24 - 25), **a drain electrode as the second electrode** (drain electrode 502, disclosed in col. 14, line 25), **and a gate electrode** (gate electrode 103, disclosed in col. 8, line 13), **wherein the source, drain and gate electrodes are formed from electro-deposited metal** (col. 8, lines 13 - 16 disclose the gate to be formed of various metals, and col. 11, lines 58 – 62 disclose the source and drain electrodes are made of titanium and aluminum. Regarding the limitation "*electro-deposited*", the patentability of a product does not depend on the method of production. See MPEP 2113. The electrode components are metal and therefore anticipate the structural limitation, regardless of how that structure is formed); **and**

wherein the first layer comprises the source electrode and the drain electrode (e.g. as seen in the figures, source electrode 501 and drain electrode 502 reside the in first layer which comprises the source and drain electrodes) **and the gate electrode lies in a fourth layer between the second layer and**

the third layer (e.g. gate electrode 103 lies in fourth layer 105, as seen in figure 1A, which is between the second layer comprising 503 and 111, and the third layer 101), **the semiconductor device further comprising a fifth layer, comprising a continuous dielectric layer, between the fourth layer and the third layer** (fifth layer 102, which is between the fourth layer 105 and third layer 101, as seen in figure 1A. Col. 8, lines 3 – 4 disclose the layer to be an insulating layer).

b. Regarding claim 7, **Yamazaki discloses a semiconductor device as claimed in claim 1, wherein the semiconductor material is embedded in the device and overlain by the first layer** (e.g. as seen in figures 5A and 5B, the semiconductor material comprising semiconductor layer 503 and the remaining semiconductor layer 111 (e.g. figure 2A) is embedded in the device, and is overlain by the first layer comprising first and second electrode components 501 and 502).

c. Regarding claim 14, **Yamazaki discloses a semiconductor device as claimed in claim 1, wherein the source and drain electrodes each partially overlap the gate electrode** (e.g. as seen in figure 5B, the source and drain electrodes 501 and 502 overlap the gate electrode 103) **but are separated therefrom by the semiconductor material and a second dielectric layer** (e.g. as seen in figure 5B, the source and drain electrodes 501 and 502 are separated

from the gate 103 by the semiconductor material 503 and a second dielectric layer 106, as disclosed in figure 106 and col. 8, line 30).

d. Regarding claim 24, **Yamazaki discloses a substrate for a display device comprising a plurality of semiconductor devices as claimed in claim 1** (e.g. figure 12A - 15D, and disclosed in Embodiment 10, col. 20, line 19).

6. Claims 18, 19, 22, and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Noguchi et al (US 5,183,780, prior art of record).

a. Regarding claim 18, **Noguchi discloses a semiconductor device** (e.g. figure 4G) **comprising:**

a first electrode component (source electrode comprising parts 26 (left side) and 28);

a second electrode component (drain electrode comprising parts 26 (right side) and 29);

a first layer comprising at least a portion of the first electrode component and at least a portion of the second electrode component (e.g. top layer comprising first and second electrode components 28, 29, and 30, formed in figure 4F from layer 27);

a second layer having a portion comprising deposited semiconductor material contacting the first and second electrode

components (semiconductor material 21 and contacts 26, disclosed in col. 7, line 39); **and**

a third layer comprising a substrate (substrate 20),

wherein the first, second and third layers are arranged in order such that the second layer is positioned between the first layer and the third layer (e.g. as seen in figure 4G, second layer 21 is between first layer comprising components 28 and 29, and third layer 20) **and**

wherein the first and second electrode components comprise electro-deposited metal (col. 8, lines 18 – 23 disclose the first and second electrode components (source and drain electrodes) comprise aluminum. Regarding the limitation "*electro-deposited*", the patentability of a product does not depend on the method of production. See MPEP 2113. The electrode components comprise metal (aluminum) and therefore anticipate the structural limitation, regardless of how that structure is formed),

wherein the device is a thin film transistor (e.g. as disclosed in col. 7, line 36) **having a channel in the semiconductor material** (e.g. channel region in semiconductor layer 21 between drain and source electrodes 26), **a source electrode as the first electrode** (source electrode 28, disclosed in col. 8, line 21), **a drain electrode as the second electrode** (drain electrode 29, disclosed in col. 8, line 22), **and a gate electrode** (gate electrode 30, disclosed in col. 8, line 22),

wherein the source, drain and gate electrodes are formed from electro-deposited metal (col. 8, lines 18 – 23 disclose the source, drain, and gain electrodes are formed from aluminum. Regarding the limitation "*electro-deposited*", the patentability of a product does not depend on the method of production. See MPEP 2113. The electrode components comprise metal (aluminum) and therefore anticipate the structural limitation, regardless of how that structure is formed), **and**

wherein the first layer comprises a first portion of the source electrode, a first portion of the drain electrode and the gate electrode (e.g. as seen in figure 4, and cited above with respect to claim 1, the first layer comprises the portions of the source electrode 28, portions of the drain electrode 29, and the gate electrode 30).

b. Regarding claim 19, **Noguchi discloses a semiconductor device as claimed in claim 18, wherein the second layer comprises a second portion of the source electrode contacting the semiconductor material and a second portion of the drain electrode contacting the semiconductor material** (e.g. as seen in figure 4, and cited above with respect to claim 1, the second layer comprises portions of the source and drain electrode (contact portions 26), which contact the semiconductor material 21).

c. Regarding claim 22, **Noguchi discloses a semiconductor device as claimed in claim 18, further comprising dielectric material in the second layer between the semiconductor material and the gate electrode in the first layer** (dielectric material 22, disclosed in col. 7, line 40).

d. Regarding claim 23, **Noguchi discloses a semiconductor device as claimed in claim 18, wherein the first layer has a substantially planar surface forming a surface of the semiconductor device incorporating portions of the source, drain and gate electrodes** (e.g. as seen in figure 4G, and disclosed in col. 8, lines 20 - 23, the first layer comprises portions 28 of the source, 29 of the drain, and 30 of gate, which are substantially coplanar with each other).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Aratani et al. (US 5,705,826, prior art of record).

a. Regarding claim 5, **Yamazaki discloses a semiconductor device as claimed in claim 1, as cited above, but is silent with respect to disclosing**

the deposited semiconductor material comprises organic semiconductor material. Yamazaki discloses the semiconductor material to be made of silicon (e.g. col. 8, line 34, with respect to figures 1A - 2C).

Aratani discloses a thin film transistor semiconductor device (e.g. figure 1), **wherein the deposited semiconductor material comprises organic semiconductor material** (e.g. as disclosed in col. 6, lines 35 - 36, col. 8, lines 36 - 37, col. 10, lines 49 - 51 (Synthesis Example 1), and col. 11, lines 11 - 13).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Yamazaki such that the semiconductor material comprises organic semiconductor material since Yamazaki discloses the semiconductor layer to be made of silicon, and Aratani discloses similar devices may comprise organic semiconductor layers instead of silicon semiconductor layers (e.g. as discussed in col. 1, lines 12 – 19 of Aratani). One would have been motivated to use organic semiconductor layers in order to make a more cost-effective device (as discussed by Aratani in col. 1, lines 12 - 19).

b. Regarding claim 8, **Yamazaki discloses a semiconductor device as claimed in claim 1, as cited above, but is silent with respect to disclosing the substrate is flexible. Yamazaki discloses the substrate to be made of glass** (e.g. col. 8, line 5).

Aratani discloses a thin film transistor semiconductor device (e.g. figure 1)**, wherein the substrate is flexible** (e.g. col. 6, lines 10 – 19 disclose the substrate may be made of glass, plastic, polyimide, and other materials).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Yamazaki such that the substrate was flexible since Yamazaki discloses the substrate to be made of glass, and Aratani discloses similar devices may comprise substrates made of either glass or plastic. It is well-known in the art that plastic is a flexible material. One would have been motivated to have a flexible substrate in order to have a device that will yield to physical shock and stress without resulting in damage to the device substrate.

Double Patenting

9. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

10. Claims 18, 19, 22, and 23 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 2, 5, 9, and 25 of copending Application No. 10/563,679. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims of the copending application disclose all of the structural limitation of the cited claims of the current application, including the first, second, and third layers, the source, drain, and gate metal electrodes, the semiconductor material, the insulating layer between the semiconductor material and gate electrode, and the relative relationships and positions between all of the claimed structures.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Response to Arguments

11. Applicant's arguments filed on June 17, 2009 have been fully considered but they are not persuasive. At present, the prior art of Yamazaki et al. and Noguchi et al. remains commensurate to the scope of claims 1 and 18, respectively, as stated by the Applicant within the context of the claim language and as broadly interpreted by the Examiner [MPEP 2111], which is elucidated and expounded upon above.

a. Regarding claim 1, the Applicant argues that Yamazaki does not disclose the limitation "*wherein the source, drain and gate electrodes are formed from*

electro-deposited metal". The Examiner reminds the Applicant that claim 1 is directed to a product, and as such, the patentability of a product does not depend on the method of its production. See MPEP 2113. Since claim 1 is directed to metal electrodes that form the source, drain, and gate electrodes, the process of forming the metal electrodes, such as through electro-deposition of metal, does not carry patentable weight. Indeed, Yamazaki discloses the source, drain, and gate electrodes to be formed of a metal (e.g. col. 8, lines 13 - 16 disclose the gate to be formed of various metals, and col. 11, lines 58 – 62 disclose the source and drain electrodes are made of titanium and aluminum), and as such, the structure of the claimed invention is anticipated, regardless of *how* that structure is formed.

b. Regarding claim 18, the Applicant argues that Noguchi does not disclose "*a second layer having a portion comprising deposited semiconductor material contacting the first and second electrode components*". The Examiner respectfully disagrees. As cited above with respect to claim 18, the Examiner interprets the first electrode *component* to comprise left side of layer 26 and layer 28, and the second electrode *component* to comprise the right side of layer 26 and layer 29 (e.g. as seen in figure 4G of Noguchi). Furthermore, the Examiner interprets the semiconductor material to be layer 21 (col. 7, line 39). With such an interpretation, Noguchi clearly shows in figure 4G that the semiconductor material 21 contacts both the left side of layer 26 and the right side of layer 26.

Since the Examiner interprets the left side of layer 26 to be part of the first electrode component and the right side of layer 26 to be part of the second electrode component, Noguchi discloses that semiconductor material 21 is in contact with both the first and second electrode components (e.g. layer 26).

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is (571)270-3899. The examiner can normally be reached on Monday - Thursday (9am - 6pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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